Marked-up Version of Claim Showing Changes

21. (twice amended) A method of constructing a multi-chip package, comprising:

placing a first chip package on a first shelf;

electrically attaching said first chip package to a plurality of shelves with direct connections between said first chip package and said plurality of shelves;

placing a second chip package on a second shelf wherein said second shelf is stacked above said first shelf; and

electrically attaching said second chip package to said second shelf with direct connections between said second chip package and said second shelf.

Marked-up Version of the Specification Showing Changes

Please replace the first full paragraph on page 11 beginning on line 9 of the specification with the following paragraph:

Once the CPU die 26 and its supporting slug 24 have been attached to the ceramic package 17, the CPU die 26 is electrically connected to the package 17 via wire bonds I 28 and 30 (step 52). Note the fabrication of a standard ceramic PGA package having a CPU device bonded to a plurality of shelves would end here. The partially fabricated chip package 10 could easily be tested for functionality at [the] this point. However, testing at this point is purely optional.